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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,146	11/18/2003	Geun-Hee Cho	8021-180 (SS-18400-US)	5288

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
07/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,146	CHO ET AL.	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6-15-07 (RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,14,15,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19* is/are allowed.

6)☒ Claim(s) *1, 2, 4, 14, 15 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6-15-07 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 14, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Iwamoto et al reference (US Patent 6,292,040) in view of the McCune reference (US Patent 5,306,971) and further in view of the Kunanayagam et al reference (US Patent 6,850,106).

Iwamoto discloses a delay-locked loop (DLL, figure 17) for receiving an external clock signal (EXTCLK) and synchronizing a phase of a feedback clock signal (INTCLK2) with a phase of the external clock signal (EXTCLK), the delay-locked loop comprising: a phase detector 16 for comparing the phase of the external clock signal with the phase of the feedback clock signal (this is a function of a phase comparator in a DLL circuit) and outputting a phase difference as an error control signal (UP/DOWN); a delay line 2, comprising a plurality of delay cells (figure 18) for receiving the external clock signal (EXTCLK), controlling the phase of the

external clock signal to obtain an output clock signal (by adjusting the delay time using shift register 4) and outputting the output clock signal (INTCLK1), wherein the number of delay cells in operation is adjusted in response to a shift signal (the shift signal is generated by the shift register 4); and a filter unit (shift register 4) for generating the shift signal for selecting the number of delay cells in operation in the delay line, in response to the error control signal (UP/DOWN).

Iwamoto does not explicitly disclose the plurality of delay cells in the delay line 2 having various unit time delays as called for in the claim.

McCune explicitly discloses a delay line (figure 1) which comprises a plurality of delay cells G1,..., G3 wherein the delay cells are structured such that the unit time delay gradually increases from the front end to the rear end of the delay line (G1 < G2 <G3, column 3, line 12) wherein delay cell is a differential amplifier (figure 4, column 4, lines 46-47). The resistance value, which is formed by transistor Q3 and resistor R1 in parallel and connected to GND, is adjusted by the collector current of transistor Q1 which in turn controlled by choosing number of diodes Q14 and Q15 (col., 5, lines 36-41) to vary resistance of each delay cell (e.g., time delay of a differential delay cell is disclosed in figure 2 of Kunanayagam). He further explicitly discloses that using such a structure of a delay line, very fine resolution in the range of one picosecond or a few picoseconds can be achieved (column 1, line 67-68).

It would have been obvious to one skilled in the art at the time of the invention was made to use the delay line taught by McCune in the Iwamoto's DLL circuit for applications which require a precise tuning of the clock signal since the McCune's delay line is capable of allowing very fine resolution adjustments.

As to claim 2, the recited limitation is disclosed in column 3, line 12 of McCune.

As per claim 4, the recited limitation is met because depending on the binary control signals, the collector current of transistor Q1 is changed.

As to claims 14-15 and 18, these claims are rejected for the same reasons noted in the rejections of claims 1-2 and 4.

Response to Arguments

4. Applicant's arguments filed 3-19-07 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Iwamoto does not disclose a specific structure of a variable delay cell in his invention in which any specific structured variable delay cell can be employed as long as there is a proper motivation to combine as such. McCune provides a variable delay cell whose structure is almost meet the requirement of claim (e.g., each delay cell in McCune has different resistances by means of combining fixed resistivity of resistor and resistance of transistor on each cell wherein the recitation of claim calls for each resistor of each delay cell has different resistance). Kunanayagam discloses a variable delay cell in which resistivity of each cell can be achieved by employing one of various known electronics component (i.e., resistor, transistor, inductor and the likes). Therefore, it would have been obvious to one skilled in the art to replace a combo of

electronics device with a single electronics device in which resistivity can be maintained. It is noted that the time delay on each delay cell is determined by changing resistivity within the delay cell.

Examiner provides motivation for each case of combining arts. Therefore, the recitation of claims 1 and 14 reads on the combined teachings of Iwamoto, McCune and Kunanayagam.

Allowable Subject Matter

5. Claim 19 is allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claim. Specifically, none of the prior art teaches or fairly suggest the limitation "a delay line, comprising a plurality of delay blocks, each delay block comprising a plurality of delay cells having the same unit time delay, wherein the unit time delay of delay cells from different delay blocks are different, the delay line for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the output clock signal, wherein the number of delay cells in operation is adjusted in response to a shift signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistors of the delay cells from different delay blocks have different resistances and the resistors of the delay cells from the same delay block have the same resistance, to vary the unit time delay" as recited in claim.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

An T. L:uu
6-29-07

Kenneth B. Wells
Primary Examiner